IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 1-12 were cancelled in a previous response.

Claims 1-12 (Cancelled)

Claims 13-44 (Cancelled)

45. (previously presented) A memory controller, comprising:

a) a host side region to be clocked by a first clock, said host side region comprising:

(i) a queue to queue command packet chunks;

(ii) a plurality of memory command packet chunk output lanes stemming from steering circuitry, said steering circuitry to guide specific command packet chunks received from said queue to specific command packet chunk output lanes, said queue having an output for each output lane, said steering circuitry further comprising:

a) a first multiplexer having a first input to receive a first packet chunk from a queue output, said first multiplexer having a second input coupled to a latch circuitry output, said latch circuitry

downstream from said queue output to hold a second packet chunk from said queue output;

b) a second multiplexer having a plurality of inputs, one of said inputs coupled to said first multiplexer's output, other inputs of said second multiplexer downstream from outputs of said queue other than said queue output; and,

b) a memory side region to be clocked by a second clock, said memory side region comprising:

inputs coupled to said memory command packet chunk output lanes.

46. (previously presented) The memory controller of claim 45 further comprising shift logic on said memory side region to receive memory command packet chunks from said memory side region inputs.

47. (previously presented) The memory controller of claim 45 wherein said steering circuitry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

48. (previously presented) The memory controller of claim 45 wherein said steering circuitry is to guide specific row command packet chunks to said specific

command packet chunk output lanes, said queue to queue row command packet chunks.

49. (previously presented) The memory controller of claim 45 further comprising a third multiplexer having a first input coupled to said queue output and a second input coupled to a path that propagates command packets chunks that do not enter said queue, said latch circuitry coupled to said third multiplexer's output to receive command packet chunks from said third multiplexer's output.

50. (previously presented) The memory controller of claim 49 wherein said third multiplexer further comprises a third input coupled to an output of said latch circuitry.

51. (previously presented) The memory controller of claim 45 wherein said steering circuitry further comprises a third multiplexer having a first input coupled an output of said second multiplexer, said third multiplexer having a second input coupled to a path that propagates command packets chunks that do not enter said queue.

52. (previously presented) The memory controller of claim 51 further comprising logic circuitry between said third multiplexer and an output lane to insert a null packet chunk onto said output lane.

53. (previously presented) An apparatus, comprising:

a memory controller, comprising:

a) a host side region to be clocked by a first clock, said host side region comprising:

(i) a queue to queue command packet chunks;

(ii) a plurality of memory command packet chunk output lanes stemming from steering circuitry, said steering circuitry to guide specific command packet chunks received from said queue to specific command packet chunk output lanes, said queue having an output for each output lane, said steering circutry further comprising:

a) a first multiplexer having a first input to receive a first packet chunk from a queue output, said first multiplexer having a second input coupled to a latch circuitry output, said latch circuitry downstream from said queue output to hold a second packet chunk from said queue output;

b) a second multiplexer having a plurality of inputs, one of said inputs coupled to said first multiplexer's output, other inputs of said second multiplexer downstream from outputs of said queue other than said queue output;

b) a memory side region to be clocked by a second clock, said memory side region comprising:

inputs coupled to said memory command packet chunk output lanes; and,

DRAM memory coupled to said memory side region of said memory controller.

54. (previously presented) The apparatus of claim 53 further comprising shift logic on said memory side region to receive memory command packet chunks from said memory side region inputs.

55. (previously presented) The apparatus of claim 53 wherein said steering circuitry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

56. (currently amended) The apparatus of claim 53 wherein said steering circuitry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

57. (previously presented) The apparatus of claim 53 further comprising a third multiplexer having a first input coupled to said queue output and a second input coupled to a path that propagates command packets chunks that do not enter said

queue, said latch circuitry coupled to said third multiplexer's output to receive command packet chunks from said third multiplexer's output.

58. (previously presented) The apparatus of claim 57 wherein said third multiplexer further comprises a third input coupled to an output of said latch circuitry.

59. (previously presented) The apparatus of claim 53 wherein said steering circuitry further comprises a third multiplexer having a first input coupled an output of said second multiplexer, said third multiplexer having a second input coupled to a path that propagates command packets chunks that do not enter said queue.

60. (previously presented) The apparatus of claim 59 further comprising logic circuitry between said third multiplexer and an output lane to insert a null packet chunk onto said output lane.

COMMENTS

The enclosed is responsive to the Examiner's Office Action mailed on May 20, 2004. At the time the Examiner mailed the Office Action claims 13-60 were pending. By way of the present response the Applicants have: 1) cancelled claims 13-44; 2) added no claims; and 3) amended claim 56. As such, claims 45-60 are now pending. The Applicants respectfully request reconsideration of the present application and the allowance of all pending claims.

Allowable Subject Matter

The Examiner has allowed claims 45-60. Applicants thank the examiner and accept the allowance of these claims.